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Description

[METHOD OF FABRICATING A POLYSILICON THIN FILM]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no. 92115200, filed June 05, 2003.

BACKGROUND OF INVENTION

[0002] Field of the Invention

[0003] This invention generally relates to a method of fabricating a thin film transistor liquid crystal display ("TFT-LCD"), and more particularly to a method of fabricating a polysilicon thin film for the thin film transistor array in the liquid crystal display.

[0004] Description of the Related Art

[0005] Polysilicon and amorphous silicon are two types of materials used for fabricating TFT for active matrix LCD panel. Polysilicon TFT has a higher aperture rate and a lower cost than the amorphous silicon TFT. The larger and uniform

silicon grains of polysilicon allow electrons to flow more freely than through amorphous silicon, which is made up of smaller and random sized silicon grains. It allows the normally external driver chips to be fabricated on the glass substrate that dramatically reduces row and column connections. Hence, polysilicon TFT technology can effectively reduce the device size in order to achieve higher integration. Generally, the requirements for mass production of polysilicon TFT are low temperature polysilicon ("LTPS") technology (450-550^{o}C), low temperature film-forming technology for the isolating film of gate terminal, and ion implantation for large area.

[0006] For application to active matrix liquid crystal displays, a low temperature process for the production of polycrystalline silicon is required to permit the use of inexpensive glass substrates. This would allow the integration of drive electronics into the display panel. Current low temperature processes include solid phase crystallization ("SPC") and excimer laser crystallization ("ELC"). Solid phase crystallization requires high temperatures (600^{o}C) and the result of the crystallization is not very well. Excimer laser crystallization technology applies the excimer laser in excimer laser crystallization or excimer laser annealing

("ELA") process to fuse the amorphous silicon thin film and make it recrystallize to a polysilicon thin film.

[0007] Because the ELC process can be carried out at a temperature lower than 450°C , resulting in a higher electron migration rate and a lower leakage current than the SPC process, and therefore it can be applied to an inexpensive glass substrate. Therefore, the production costs can be reduced.

[0008] FIGs.1A-1B show the fabrication process of a conventional polysilicon thin film. Referring to FIG.1A, a substrate 100 having an isolating layer 102 formed thereon is provided. Then a smooth amorphous silicon layer 104 is formed on the isolating layer 102. After the amorphous silicon layer 104 is deposited, the excimer laser 106 with enough energy is applied to substantially fuse the amorphous silicon layer 104; i.e., there are some unfused silicon grains left on the surface of the isolating layer 102 as discrete seeds (not shown in FIG.1A).

[0009] Referring to FIG.1B, the fused amorphous silicon layer 104 uses the unfused silicon grains as discrete seeds to crystallize into a polysilicon layer 108, which is used for drain region, source region, and channel region of the TFT.

[0010] The conventional process of forming polysilicon thin films

has to precisely control the power of the excimer laser in order to make some unfused amorphous silicon grains left as discrete seeds for better crystallization. However, the excimer laser is a pulsed laser. The power density of each pulse would be different and thus is difficult to control. As a result, the size of silicon grains left would be different; the silicon grains would comprise protrusions at their boundaries reflecting a poor smoothness of the polysilicon thin film, which would adversely affect the TFT devices.

SUMMARY OF INVENTION

[0011] An object of the present invention is to provide a method of fabricating a polysilicon thin film for forming a bigger silicon grain and reducing the amount and the density of the protrusions in order to achieve a smoother polysilicon thin film for the TFT devices.

[0012] The present invention provides a method of fabricating a polysilicon thin film, comprising: forming a first solid phase silicon layer on a substrate, wherein said solid phase silicon layer has a plurality of first protrusions with different heights, wherein the maximum distance between the top of said first protrusions and the surface of said substrate is X_1, and the minimum distance between the

top of said first protrusions and the surface of said substrate is Y_1; liquidizing a portion of said first solid phase silicon layer to liquidize a thickness of Z_1 of said first solid phase silicon layer, wherein $Y_1 < Z_1 < X_1$, and a portion of said first protrusions having a distance which is between the top of said first protrusions and the surface of said substrate and larger than Z_1 is not liquidized and become a plurality of silicon grains; and performing crystallization using said silicon grains as crystalline seeds. The present invention also provides a method of fabricating a polysilicon thin film, comprising: forming a first polysilicon layer on a substrate, wherein said first polysilicon layer has a plurality of first protrusions with different heights, and the maximum distance between the top of said first protrusions and the surface of said substrate is X_2, and the minimum distance between the top of said first protrusions and the surface of said substrate is Y_2; etching a portion of said first polysilicon layer to remove said first protrusions and said first polysilicon layer having a thickness of Z_2 to form a plurality of second protrusions on said substrate, wherein $Y_2 < Z_2 < X_2$ and the number of said second protrusions is less than the number of said first protrusions; forming a first amorphous silicon layer on said

substrate and said second protrusions; and performing a first annealing process to crystallize to form a second polysilicon layer by using said second protrusions as crystalline seeds.

[0013] Accordingly, the present invention uses higher protrusions of an initially formed silicon layer as crystalline seeds for the subsequent crystallization step so that the newly-formed polysilicon thin film has smoother and bigger silicon grains, and has lesser density of protrusions. Furthermore, the polysilicon thin film of the present invention can be applied to form polysilicon thin film transistors or other devices.

[0014] The above is a brief description of some deficiencies in the prior art and advantages of the present invention. Other features, advantages and embodiments of the invention will be apparent to those skilled in the art from the following description, accompanying drawings and appended claims.

Brief Description of Drawings

[0015] FIGs.1A-1B show the fabrication process of a conventional polysilicon thin film.

[0016] FIGs.2A-2F are the cross-sectional views of a process of fabricating a polysilicon thin film in accordance with a first

embodiment of the present invention.

[0017] FIGs.3A-3G are the cross-sectional views of a process of fabricating a polysilicon thin film in accordance with a second embodiment of the present invention.

[0018] FIG.4 shows the distribution of protrusion height vs. protrusion amount of the polysilicon layer in FIG.2C and FIG.3C in accordance with the present invention.

DETAILED DESCRIPTION

[0019] *<First embodiment>*

[0020] FIGs.2A-2F are the cross-sectional views of the first embodiment of the process of fabricating a polysilicon thin film in accordance with the present invention.

[0021] Referring to FIG.2A, a substrate 200 is provided; the substrate 200 can be a silicon substrate, a glass substrate or a plastic substrate. Then an isolating layer 202 is formed on the substrate 200; the isolating layer material may include silicon dioxide. The isolating layer 202 can be formed by a low pressure chemical vapor deposition ("LPCVD"), a plasma enhanced chemical vapor deposition ("PECVD") or a sputter. Next, an amorphous silicon layer 204 is formed on the isolating layer 202; the amorphous silicon layer 204 can be formed by a LPCVD, a PECVD or a

sputter, wherein amorphous silicon layer 204 has a thickness of D1 approximately between 1nm and 1000nm.

[0022] Referring to FIG.2B, a first annealing process 206 is performed, wherein the first annealing process 206 is performed by applying excimer laser to the amorphous silicon layer 204 to fuse most part of the entire amorphous silicon layer 204 but there would be some amorphous silicon grains 207 left on the surface of the isolating layer 202 as the crystallization seeds (nucleation site) for crystallization.

[0023] Referring to FIG.2C, the fused portion of the amorphous silicon layer 204 uses the unfused amorphous silicon grains 207 as crystallization seeds to crystallize and then a polysilicon layer 208 having a thickness of D2 is formed; wherein D2 is approximately between 1nm and 1000nm. As shown in FIG.2C, during the crystallization process, the silicon grains will continue to grow laterally until they contact to the neighboring silicon grains. Furthermore, the boundary 210 between the silicon grains will become protrusions 212 because the neighboring silicon grains push against each other. Generally, the heights of those protrusions 212 will distribute in a different waybased on the distance between the two neighboring silicon grains,

the temperature of the amorphous silicon layer 204 after the excimer laser is applied, or the growth rate of the silicon grains.

[0024] Referring to FIG.2D, an amorphous silicon layer 214 is formed on the crystallized polysilicon layer 208; the amorphous silicon layer 214 can be formed by a LPCVD, a PECVD or a sputter, wherein the amorphous silicon layer 214 has a thickness of D3; wherein D3 is approximately between 1nm and 1000nm. Furthermore, as shown in FIG.2D, the amorphous silicon layer 214 also has protrusions 215 corresponding to the protrusions 212. Among those protrusions 215, the maximum distance between the top of the protrusions 215 and the isolating layer 202 is X_1 (not shown in FIG.2D), and the minimum distance between the top of the protrusions 215 and the isolating layer 202 is Y_1 (not shown in FIG.2D).

[0025] As shown in FIG. 2C and FIG.2E, a second annealing process 218 is performed, wherein the second annealing process 218 can be performed by applying the excimer laser to a portion of the amorphous silicon layer 214 to liquidize the amorphous silicon layer 214 and the polysilicon layer 208 to become a liquid silicon layer 220; there are still some unfused silicon grains 222 left on the surface of

the isolating layer 202. The energy density of the excimer laser depends on the heights of the amorphous silicon layer 214, the polysilicon layer 208, and the protrusions 215. By controlling the energy density of the excimer laser, a thickness lower than Z_1 of the amorphous silicon layer 214 and the polysilicon layer 208 is fused in part, wherein $Y_1 < Z_1 < X_1$. At the same time, the portion of the protrusions 215 with the distance, which is between the top of the protrusions 215 and the substrate 200 and higher than Z_1, are not fused completely and become a plurality of silicon grains 222. The number of the silicon grains222 is less than that of the protrusions 212.

[0026] The protrusions 215 having a distance less than Z_1, between the top of the protrusions 215 and the isolating layer 202, will be totally fused by the excimer laser, but the protrusions 215 having a distance more than Z_1, between the top of the protrusions 215 and the isolating layer 202, will become the silicon grains 222. This is because the polysilicon layer 208 with a thickness of $(X_1 - Z_1)$ can be unfused.

[0027] Referring to FIG.2F, the crystallization process is performed. The liquid silicon layer 220 uses the silicon grains 222 as crystalline seeds to form the polysilicon layer 224.

[0028] *<Second embodiment>*

[0029] FIGs.3A-3G are the cross-sectional views of a process of fabricating a polysilicon thin film in accordance with a second embodiment of the present invention.

[0030] Referring to FIG.3A, a substrate 300 is provided; the substrate 300 can be a silicon substrate, a glass substrate or a plastic substrate. Then an isolating layer 302 is formed on the substrate 300; the isolating layer material can be silicon dioxide. The isolating layer 302 can be formed by using a LPCVD, a PECVD or a sputtering method. Later, an amorphous silicon layer 304 is formed on the isolating layer 302; the amorphous silicon layer304 can be formed by using a LPCVD, a PECVD or a sputtering method, wherein amorphous silicon layer 304 has a thickness of D4; wherein D4 is approximately between 1nm and 1000nm.

[0031] Referring to FIG.3B, a first annealing process 306 is performed, wherein the first annealing process 306 is performed by applying excimer laser to the amorphous silicon layer 304 to fuse most of the amorphous silicon layer 304 but there would be some amorphous silicon grains 307 left on the surface of the isolating layer 302 as the crystallization seeds (nucleation site) for crystallization.

[0032] Referring to FIG.3C, the fused portion of the amorphous silicon layer 304 uses the unfused the amorphous silicon grains 307 as crystallization seeds to crystallize and then form a polysilicon layer 308 having a thickness of D5; wherein D5 is approximately between 1nm and 1000nm. As shown in FIG.3C, during the crystallization process, the silicon grains will continue to grow laterally until they come in contact with the neighboring silicon grains. Furthermore, the boundary 310 between the silicon grains will form protrusions 312 because the neighboring silicon grains push against each other. Generally, the heights of those protrusions 312 will distribute in a different way based on the distance between the two neighboring silicon grains, the temperature of the amorphous silicon layer 304 after the excimer laser is applied, or the growth rate of the silicon grains. Among those protrusions 312, the maximum distance between the top of the protrusions 312 and the isolating layer 302 is X_1 (not shown in FIG.3C), and the minimum distance between the top of the protrusions 312 and the isolating layer 302 is Y_1 (not shown in FIG.23C).

[0033] Referring to FIG.3D, an etching process 314 is performed to remove the portion of polysilicon layer 308 having a

thickness less than Z_2, wherein the etching is performed by using an anisotropic etching and $Y_2 < Z_2 < X_2$.

[0034] The polysilicon layer 308 with the protrusions 312 having a distance, which is between the top of the protrusions 312 and the substrate 300 and less than Z_2, will be etched, but the polysilicon layer 308 with the protrusions 312 having a distance, which is between the top of the protrusions 312 and the substrate 300 and more than Z_2, will not be totally etched to form the silicon grains 315 on the surface of the substrate 300. The number of the silicon grains 315 is less than that of the protrusions 312.

[0035] Referring to FIG.3E, an amorphous silicon layer 316 is formed by a LPCVD, a PECVD or sputtering method, wherein the amorphous silicon layer 316 has a thickness of D3, which is approximately between 1nm and 1000nm. Furthermore, as shown in FIG.3D, the amorphous silicon layer 316 also has protrusions 317 corresponding to the protrusions 315.

[0036] Referring to FIG.3F, a second annealing process 318 is performed, wherein the second annealing process 318 is performed by applying the excimer laser to the amorphous silicon layer 316 to liquidize the amorphous silicon layer 316 to become a liquid silicon layer 320; there are

unfused silicon grains 315 left on the surface of the isolating layer 302. The energy density of the excimer laser is controlled not to fuse the entire silicon grains 315 so that silicon grains 315 can be used as crystalline seeds.

[0037] Referring to FIG.3G, the crystallization process is performed. The liquid silicon layer 320 uses the silicon grains 315 as crystallization seeds to form the polysilicon layer 324.

[0038] In the first embodiment of the present invention, the polysilicon layer 208 and the amorphous silicon layer 214 in FIG.2D can be deemed to be solid phase silicon layers; the excimer laser annealing process 218 to the amorphous silicon layer 214 in FIG.2E can be deemed to be a liquidization process to the solid phase silicon layer.

[0039] Moreover, in the second embodiment of the present invention, the etching process 314 applied to the polysilicon 308 and the excimer laser annealing process 318 applied to the amorphous silicon layer 316 in FIG.3D and FIG.3F respectively can be deemed to be liquidization processes.

[0040] FIG.4 shows the distribution of protrusion amount vs. protrusion height of the polysilicon layer in FIGs.2 and FIG.3 in accordance with the present invention. According to FIG.4, this curve is Gaussian distribution; i.e., for the

protrusions, the more the heights get close to the average value, the larger the amount is. The present invention thus provides a way to grow bigger silicon grains and to produce fewer protrusions by rejecting the protrusions having a specific height. (e.g., the left side of S1 in FIG.4) Then the present invention uses the remaining protrusions as crystallization seeds to grow bigger silicon grains to produce fewer protrusions. Hence, the method of the present invention provides a smoother polysilicon thin film for the TFT devices and can be applied to form thin film transistors for better electron mobility and less current leakage.

[0041] Accordingly, the present invention has the following advantages.

[0042] 1. By applying an excimer laser annealing to an amorphous silicon layer deposed on a crystallized polysilicon, the amount and the density of the protrusions on the polysilicon layer can be effectively reduced. Next, the residual protrusions (silicon grains) are used as crystallization seeds to form a polysilicon layer having bigger silicon grains and better surface smoothness.

[0043] 2. By etching the crystallized polysilicon layer and then depositing an amorphous silicon layer on it and perform-

ing the excimer laser annealing process, the protrusions of the polysilicon layer can be effectively reduced. The residual protrusions (silicon grains) then are used as crystalline seeds to form a polysilicon layer having a better surface smoothness.

[0044] 3. The polysilicon thin film formed by the first and second embodiments can provide better electron mobility and less current leakage. Furthermore, the polysilicon thin film of the present invention also can be applied in other devices such as the driver circuits of COG process.

[0045] The above description provides a full and complete description of the preferred embodiments of the present invention. Various modifications, alternate construction, and equivalents may be made by the skill in the art without changing the scope or spirit of the invention. Accordingly, the above description and illustrations should not be construed as limiting the scope of the invention which is defined by the following claims.